

High Efficient Test Methodology of Multi-Lane Serial Timing Signal

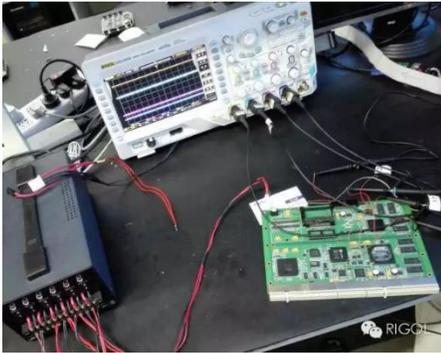


Figure 1. The testing board of Industrial controlling machine

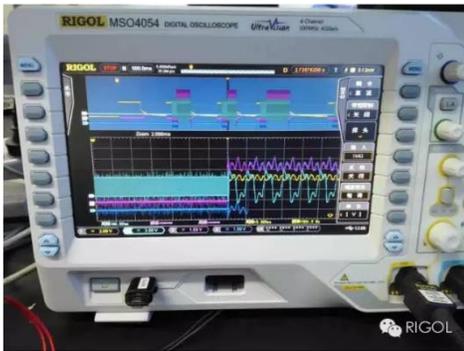


Figure 2. Serial Timing Signal Testing



Figure 3. Testing for 4 Fixed Time-Delay Signal

Rigol has contacted many customers who are in charge of industrial controlling machines and system controlling products recently, and we found that they always intend to do the multi-lane and serial timing signal testing. Generally, the number of the test lane expands to 4 to 7 lanes and the timing clock testing expands to 8 measurement lanes. Testing engineers are always frustrated to face a tough situation that oscilloscope is always equipped with maximum 4 channels, but the serial clock timing signal expands to 8 lanes and the scope couldn't satisfy the maximum channel numbers testing. If engineers separate the testing by two times, it may induce unexpected measurement errors during four by four multi-channel comparison, so it's really a tremendous challenge for test engineers to implement the serial clock timing signal testing.

We continue to communicate with test engineers and found that the signal amplitudes are different as well due to the controlling system corresponds to variable controlled equipment. So test engineers must implement not only timing comparison between different lanes but also the amplitudes and frequencies comparisons and verifications during the testing. Besides of that, the rising time and overshoot values will be also included. Engineers always adjust the electric circuit to improve the signal quality via judgment through different test parameters, so the logic analyzer just only can solve the timing comparison issue but cannot verify the signal quality directly. Finally, the test engineers should have one multi-channel oscilloscope which can expand the test capabilities up to 8 channels and efficiently solve the accuracy of different lanes timing comparison.

According to customers' request, we verify the implemented possibility and use DS4000 series oscilloscope as the best test solution. The test methodology is to generate 4 lanes pulse signals which has fixed timing delay relationship through by two oscilloscopes and observed 4 lanes timing signals on one scope. We can recognize the test result and prove its reliability.



Figure 4. Four Lanes Time Delay Diagram

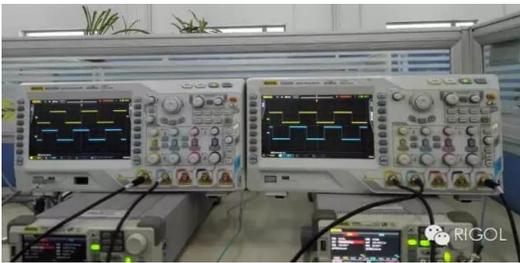


Figure 5. Testing for Both 4 Lanes Signals Via Two Oscilloscopes



Figure 6. Testing A, B Signal Timing on Oscilloscope 1



Figure 7. Testing C, D Signals Timing on Oscilloscope 2

At first we can use Rigol’s arbitrary waveform generator to generate 4 lanes pulse signals which has 2.5us timing delay lane by lane, these are represented by A, B, C, D. Then we send the four lanes signals into one oscilloscope. A signal is simulated as a clock one. Users can observe the 4 lanes signals on the oscilloscope which are correspondent to setting values. And we can say every rising edge of each signal has 250us timing delay compared to previous one.

Let us send the A, B signals into oscilloscope 1, C,D signals are sent into oscilloscope 2, and then observe the serial timing relationship between 4 signals. The two oscilloscopes should be set to synchronize the settings and make sure the serial timing relationship would be accurately displayed on two oscilloscopes.

According to the result of 4 lanes signals observed on two oscilloscopes, all the rising edges of 4 lanes signals have 2.5us timing delay compared to the reference points. It’s the same result to send 4 lanes signals simultaneously into one oscilloscope. So we can accurately measure the amplitudes, frequency...etc after synchronize the settings of multiple oscilloscopes and it can raise up the test efficiency and accuracy in advance. If users can consolidate the four lanes signal testing via one integrated testing software and displayed on one interface through two oscilloscopes, it can improve more about the engineer’s usage feeling and the habit of signal observation will not be changed.

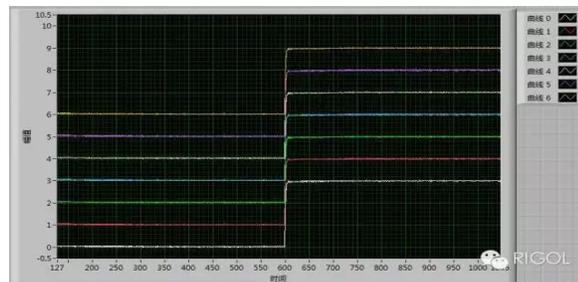


Figure 8. Synchronization on Multi-Instrument